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(54) **Method of micro-machining an integrated sensor on the surface of a silicon wafer.**

(57) A method for micro-machining the surface of a silicon substrate (10,14) which encompasses a minimal number of processing steps. The method involves a preferential etching process in which a chlorine plasma-etching is capable of laterally etching an N+ buried layer (12) beneath the surface of the bulk substrate (10,14). Such a method is particularly suitable for forming sensing devices which include a small micro-machined element (18), such as a bridge, cantilevered beam, membrane, suspended mass or capacitive element, which is supported over a cavity (22) formed in a bulk silicon substrate (10,14). The method also permits the formation of such sensing devices on the same substrate as their controlling integrated circuits. The method can optimise the dimensional characteristics of the micromachined element (18) or encapsulate the micromachined element (18).

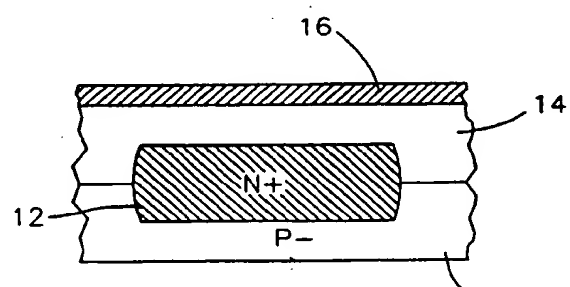


FIG.2b

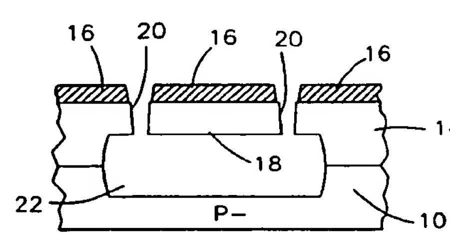


FIG.2c

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The present invention generally relates to bulk micro-machining processes used to form integrated circuit devices on or under the surface of a silicon wafer. More particularly, this invention relates to an improved method for micro-machining integrated sensor devices on the surface of a silicon wafer which incorporates bipolar and BiCMOS devices, wherein the method encompasses the formation of bridges, cantilevered beams, membranes, suspended masses, and capacitive elements within the surface of the silicon wafer.

Bulk micro-machining of silicon wafers is well known in the semiconductor arts. Generally, this process involves forming semiconductor devices on a silicon wafer by etching the bulk silicon at the surface of the wafer, in contrast to etching methods in which semiconductor devices are formed by selectively etching layers which were previously deposited on the surface of the wafer substrate. Bulk micro-machining can be used to form micro-machined features in the surface of a silicon substrate from which sensing devices can be formed, and is generally preferred over etching deposited layers in the fabrication of sensing devices in that less warpage occurs, thereby enhancing the accuracy of the sensing device. Bulk micro-machining is often conducted using a conventional wet-etch process, which is isotropic in nature. Dry-etching processes, such as plasma-etching, are becoming more common because of their capability for higher packing density as a result of being anisotropic in nature.

In the past, sensing devices have often been fabricated by stacking silicon wafers on top of each other so as to form a cavity over which a sensing micro-machined element, such as a beam, bridge or membrane, can be formed with the upper wafer. Alignment tolerances as well as sharp corners and edges on the wafers create points of stress concentration within the sensing device, which interfere with the ability of the micro-machined element to accurately detect the pressure or motion for which the device is intended. Consequently, bulk micro-machining methods are often preferred in that the residual stresses and stress concentrators common to stacked-wafer techniques can generally be avoided.

A recent example of such a bulk micro-machining method is disclosed by Zhang and McDonald (Digest IEEE Int. Conf. on Solid State Sensors and Actuators, pp. 520-523 (1991)), as generally illustrated in Figures 1a to 1f. As illustrated in Figures 1a to 1f of the accompanying drawings, Zhang and McDonald disclose thermally depositing a silicon dioxide layer 102 on an arsenic-doped n-type <100> substrate 100 which is to be bulk micro-machined. The silicon dioxide layer 102 is then photolithographically patterned using photoresist 104 which has been spun on the silicon dioxide layer 102, as indicated in Figure 1a. A plasma-etching process is then used to form trenches 106 to a depth of about 4 micrometres in the substrate 100, as shown in Figure 1b.

A second layer of silicon dioxide (not shown) is then thermally grown on all exposed surfaces, followed by the deposition of another layer of silicon dioxide 108 using plasma-enhanced chemical vapour deposition (PECVD), as shown in Figure 1c. After patterning and etching through the layers of silicon dioxide to provide a metal-to-substrate contact window, a layer of aluminium 110 is deposited on the upper layer of silicon dioxide 108, as indicated in Figure 1d, from which electrodes are patterned. An anisotropic etch is then used to remove the silicon oxide 108 from the bottom of the trenches 106, as shown in Figure 1e, and then an isotropic plasma etch is used to undercut the substrate 100 between the trenches 106 so as to form a cavity 114 beneath the surface of the substrate 100. As shown in Figure 1f, the cavity 114 creates a suspended beam 112 which is suitable for sensing motion.

The above process is likely to be suitable for many applications, in that plasma-etching techniques are capable of micro-machining small features which can be integrated onto a chip containing integrated circuitry. However, the plasma-etching process disclosed by Zhang and McDonald does not readily lend itself to forming selectively-shaped cavities, in that the isotropic nature of the plasma etch requires that the process should include a silicon dioxide deposition and etch to limit the direction of the etching action. Where no silicon dioxide layer or metal layer is present, the plasma etch will proceed uninhibited until the etching process is discontinued, as suggested by the shape of the cavity 114 shown in Figure 1f. Accordingly, the process disclosed by Zhang and McDonald requires an oxide deposition and etch after the trench has been etched to roughly define the cavity. Whilst such additional steps are entirely conventional, it is a continuous objective in the semiconductor industry to minimise the number of processing steps necessary to form any given device.

Furthermore, the disclosures of Zhang and McDonald are limited to the formation of bridges and cantilevered beams. In other words, any method by which larger structures can be formed, such as a suspended mass for motion sensing, is not disclosed. Nor do the disclosures suggest how the trenches can be suitably sealed so as to form membranes for sensing pressure or, alternatively, encapsulated so as to protect the bridge and cantilevered beams.

Thus, it would be desirable to provide an improved method for forming small, integrat d micro-

machined elements in a silicon wafer using a bulk micro-machining process, in which the method reduces the number of processing steps necessary to form the desired micro-machined elements. Furthermore, it would be desirable that such a method should be conducive to further processing by which the micro-machined elements can be adapted to form various types of sensing devices having a wide variety of possible configurations.

A method for micro-machining a surface of a silicon substrate according to the present invention is characterised by the features specified in the characterising portion of claim 1.

It is an object of this invention to provide an improved method for bulk micro-machining a silicon wafer for the purpose of forming a small feature-size micro-machined element within the silicon wafer, wherein the micro-machined element is suitable for use as a component of a semiconductor sensing device.

It is a further object of this invention that such a method should require a minimal number of processing steps to form uniform cavities and trenches which define the micro-machined element, whilst simultaneously enabling the cavities and trenches to be formed within the silicon wafer in a highly selective and controlled manner.

It is still a further object of this invention that such a method should be conducive to forming various types of sensing devices having a wide variety of physical configurations.

It is yet another object of this invention that such a method should lend itself to subsequent processing steps to further enhance the desired characteristics of the micro-machined element.

In accordance with a preferred embodiment of this invention, these and other objects and advantages are accomplished as follows.

According to the present invention, there is provided a method for bulk micro-machining the surface of a silicon substrate which encompasses a minimal number of processing steps. The method is particularly suitable for forming a sensing device that includes a small micro-machined element, such as a bridge, cantilevered beam, suspended mass, membrane or capacitive element, which is supported over a cavity formed in the silicon substrate. The method enables the formation of a wide variety of sensing devices on a single silicon wafer, as well as enabling the formation of a diverse variety of micro-machined shapes, such as a narrow bridge or a wide paddle-shaped deflectable mass. This invention also provides novel methods by which such structures can be improved, such as through optimising the dimensional characteristics of the micro-machined element or by encapsulating the micro-machined element.

The method involves forming an N+ region in the surface of a substrate, and then growing a silicon layer, such as an epitaxial silicon layer, from the surface of the substrate. As a result, the N+ region forms an N+ buried layer beneath the silicon layer. The silicon layer is then masked and plasma-etched so as to form one or more trenches through the silicon layer and into the N+ buried layer. As a result of a preferred plasma-etching method taught by this invention, the N+ buried layer can be laterally etched so as to form a cavity beneath the surface of the silicon layer. Generally, the shape of the cavity will be uniformly rounded as a result of the N+ buried layer being formed without sharp edges or corners. Furthermore, the dimensions of the cavity can be readily configured for the particular sensing application to form a micro-machined element between the cavity and the surface of the silicon layer. Depending on the sizes and shapes of the desired cavity and trenches, the micro-machined element can be formed as a bridge, cantilevered beam, deflectable mass, membrane, or capacitive element.

According to this invention, the preferred plasma etch is conducted using a chlorine-containing gas as the etchant medium. The chlorine gas is preferably held at a pressure of about 13 Pa (100 mTorr) to about 133 Pa (1000 mTorr), and the wafer is preferably stabilised at a temperature of at least about 35°C. Under these conditions, the N+ buried layer is preferentially etched, with the silicon substrate surrounding the N+ buried layer being substantially unaffected. As a result, the size and shape of the cavity can be accurately defined by appropriately defining the size and shape of the N+ buried layer. Consequently, the configuration of the micro-machined element can also be accurately predetermined, permitting the fabrication of an accurate sensing device.

Also in accordance with this invention, the micro-machined element can be further defined by depositing a polysilicon film on the element so that all, or a portion of all, the trenches are filled. With this method, the micro-machined element can be formed as a sealed reference chamber for a pressure-sensing device, a narrow cantilevered beam or a relatively large paddle-shaped mass for a motion-sensing device, or a capacitive element having a high capacitance value.

The present invention also encompasses novel methods by which the micro-machined element can be encapsulated so as to be isolated from the surrounding environment of the silicon wafer.

The above and other advantages of this invention will become more apparent from the following description taken in conjunction with the accompanying drawings, in which:

Figures 1a to 1f illustrate the prior-art bulk micro-machining processing steps disclosed by Zhang and McDonald;

Figures 2a to 2c illustrate an improved bulk micro-machining process by which a micro-machined element is defined as a result of forming a cavity beneath the surface of a silicon wafer, in accordance with this invention;

Figure 3 is a plan view of a representative motion-sensing device which can be fabricated in accordance with the bulk micro-machining process of this invention;

Figures 4a to 4c illustrate a method for sealing the cavity of Figure 2c so as to form a sealed reference chamber for a pressure-sensing device, in accordance with a preferred aspect of this invention;

Figure 5 is a further illustration of the method shown in Figures 4a to 4c, by which a deflectable mass shown in Figure 3 can be fabricated;

Figure 6 shows the pressure-sensing device shown in Figure 4c, which is fabricated adjacent the motion-sensing device shown in Figure 3, wherein each device can be formed adjacent, and on the same substrate as, the integrated circuitry used to process signals generated by the devices;

Figure 7 shows a pair of pressure-sensing devices of the type shown in Figure 4c, wherein one of the pressure-sensing devices is modified to sense pressure at the rear of the silicon wafer;

Figures 8a and 8b illustrate a method by which the process of this invention can be further modified to enhance the capacitance of a micro-machined capacitor formed in accordance with the method of this invention;

Figures 9a to 9d illustrate a method by which the process of this invention can be further modified to encapsulate the motion-sensing device shown in Figure 3; and

Figures 10a to 10c illustrate a second method by which the process of this invention can be further modified to encapsulate the motion-sensing device shown in Figure 3.

It is to be understood that ranges given herein are approximate and that the advantages described may still be obtained by going outside the ranges given, as will be apparent to the skilled person.

A method is provided by which micro-machined elements can be accurately micro-machined in bulk in the surface of a silicon wafer using a minimal number of processing steps. The bulk micro-machining method of this invention enables well-defined trenches and cavities to be formed in a silicon wafer, resulting in the formation of a micro-machined element, such as a bridge or a cantilevered beam, at or under the surface of the silicon wafer. Furthermore, the bulk micro-machining method of this invention offers an improvement over the disclosures of Zhang and McDonald in that the oxide deposition and etch step after the trenches are formed is completely eliminated. In accordance with additional methods taught by this invention, such micro-machined elements can be modified to form a membrane for a pressure-sensing device, a suspended mass for a motion-sensing device, or a parallel plate capacitor. This invention also encompasses methods by which such a micro-machined element can be encapsulated so as to be isolated from the environment surrounding the silicon wafer.

The bulk micro-machining method of this invention is a silicon surface etching process which employs a plasma-etching technique. In particular, the preferred etching technique employs an etchant medium which will preferentially attack N+ doped silicon in the form of an N+ buried layer. The parametres of the etching process are specifically selected so that the N+ buried layer will be preferentially etched while the surrounding substrate material will be substantially unaffected. As a result, by forming trenches into the substrate, a lateral etch can occur wherever a trench encounters an N+ buried layer.

As shown in Figures 2a to 2c, the preferred bulk micro-machining method of this invention begins with the creation of an N+ region 12 within a suitable substrate. The preferred method will be described in reference to fabricating micro-machined elements within a bipolar or bipolar-complementary metal-oxide-semiconductor (BiCMOS) process, though those skilled in the art will readily recognise that the use of the method of this invention can also be extended to other processes, including CMOS processes.

As shown, the N+ region 12 is preferably formed within a lightly-doped p-type substrate 10. This N+ region 12 will later form the N+ buried layer 12 mentioned above. The substrate 10 is doped with a suitable dopant, such as the ions of boron or another trivalent element, so as to have a suitable acceptor concentration, as is well known in the art. The substrate 10 represents a portion of a monocrystalline silicon wafer which is made sufficiently thick so as to permit handling, whilst the lateral dimensions of the wafer are made generally large enough such that the wafer may be subsequently diced into a number of chips.

The N+ buried layer 12 can be formed using various suitable techniques known to those skilled in the art. However, in accordance with this invention, the N+ buried layer 12 is more preferably created by donor-implanting the substrate 10 with the ions of arsenic, phosphorous, antimony or another pentavalent element. A barrier layer of silicon

oxide (not shown) having a thickness of about 800 nanometres (8000 Angstroms) is then thermally formed on the surface of the substrate 10. Using a photoresist mask (not shown) and known photolithography techniques, the barrier layer is patterned to define the region of the substrate 10 in which the N+ buried layer 12 is to be formed. The barrier layer is then etched down to the surface of the substrate 10 and the photoresist mask is stripped. The donor ions are then implanted into the substrate 10 to form the N+ region 12. The donor ions are preferably subjected to an accelerating voltage of about 100 KeV and implanted to a dosage of about $5 \times 10^{15}$ ions/cm$^2$. The substrate 10 is then heated to a temperature of about 1250°C for a duration of about 2 hours to drive the donor atoms deeper into the substrate 10. The barrier layer of silicon oxide is then removed from the surface of the substrate 10 in any conventional manner.

The resulting N+ region 12 preferably has an average concentration of greater than about $1 \times 10^{18}$ impurities/cm$^3$. As will become more apparent, the dimensional characteristics of the N+ region 12, such as its length, width and depth, can vary with the particular application, depending on the geometric configuration of the micro-machined element that is desired to be formed.

As shown in Figure 2b, an epitaxial layer 14 is then grown from the surface of the substrate 10 so as to bury the N+ region 12, thus establishing the N+ buried layer 12. The epitaxial layer 14 can be formed in a completely conventional manner, with its thickness being adjusted to the particular requirements of the application. As will be apparent to those skilled in the art, the inclusion of the N+ buried layer 12 in the substrate 10 is compatible with bipolar and BiCMOS processes which typically include an N+ buried layer under an epitaxial silicon layer. This method is also compatible with CMOS processes which do not usually include an N+ buried layer, though an additional masking step would be required to form the N+ buried layer 12.

Prior to etching, an oxide layer 16 is grown or deposited in a conventional manner on the epitaxial layer 14. The oxide layer 16 can be between about 800 nanometres (8000 Angstroms) and about 1200 nanometres (12,000 Angstroms) thick, which is sufficient to provide a protective layer to the epitaxial layer 14 during the subsequent etching process. The oxide layer 16 is patterned using a photoresist mask (not shown). A plasma etch is then used to selectively remove the oxide layer 16 from each surface region of the epitaxial layer 14 which corresponds to the desired placement of a trench. The photoresist mask is then removed and the preferred silicon surface etching process of this invention is performed.

As previously noted, the preferred etching method is a plasma-etching process which is conducted using a chlorine-containing gas or a suitable chlorine compound as the etchant medium. The preferred chlorine plasma-etching process is critical in terms of its ability to preferentially form a cavity which extends laterally beneath the surface of the epitaxial layer 14. To achieve this result, chlorine gas is preferably held at a pressure of about 13.33 Pa (100 mTorr) to about 133.32 Pa (1000 mTorr), and the substrate 10 is preferably held at a temperature of at least about 35°C, such that the chlorine plasma etching process acts to preferentially etch the N+ buried layer 12, instead of the epitaxial layer 14 and the substrate 10.

Whilst the above conditions are critical to performing the lateral etch of the N+ buried layer 12, other known and conventional etching methods can be employed to first form one or more trenches 20 through the epitaxial layer 14, as shown in Figure 2c, for the purpose of gaining access to the N+ buried layer 12. Accordingly, the present invention encompasses the chlorine plasma-etching process of this invention as well as any other foreseeable trench-etching process, for the purpose of forming trenches 20 through the epitaxial layer 14.

Once access is gained to the N+ buried layer 12 via one or more trenches 20, the preferred chlorine plasma-etching process is used to preferentially etch the N+ buried layer 12 so as to form a cavity 22 beneath the epitaxial layer 14. As shown in Figure 2c, the preferred chlorine plasma-etching process of this invention does not substantially affect either the lightly-doped epitaxial layer 14 or the substrate 10. Accordingly, the size and shape of the cavity 22 is defined by the size and shape of the N+ buried layer 12. Generally, the resulting shape of the cavity 22 will be uniformly rounded as a result of the N+ buried layer 12 being naturally formed without sharp edges or corners. Using the preferred etching process, lateral etches of up to 52 micrometres per side have been observed, which is greater than that achievable by the prior art. Furthermore, using the preferred plasma-etching process, the lateral N+ buried layer etch aspect ratio can exceed 10:1.

The portion of the epitaxial layer 14 above the cavity 22 defines a micro-machined element 18. The precise shape of the micro-machined element 18 depends on the shape and number of trenches 20 formed, the size and shape of the cavity 22, and the depth of the cavity 22 below the upper surface of the epitaxial layer 14. Thus, the precision by which the width of the micro-machined element 18 can be defined is primarily dependent on the accuracy of the trench mask, whilst the precision by which the thickness of the micro-machined element

18 can be defined is primarily dependent on the ability to accurately control the growth of the epitaxial layer 14. Typically, lateral accuracies of about 0.1 micrometres can be readily achieved using conventionally-known patterning techniques, whilst epitaxial growth can be controlled to within 5%, permitting the fabrication of a precision micromachined element 18.

By using the preferred plasma-etching technique of this invention, extremely fine micromachined elements 18 can be formed in the epitaxial layer 14. Referring to Figure 3, an illustrative example of a type of motion-sensing device 25 which can be formed with the method of this invention is shown. The micro-machined element 18 for this motion-sensing device 25 is an n-type cantilevered beam which includes two branches on which a p-type resistor 24 is formed. As illustrated, the micro-machined element 18 is supported above a large open cavity 22 and surrounded by an elongated trench 20b on three sides. Whilst the large open cavity 22 may alternatively be formed during the etching process as a trench, the cavity 22 beneath the micro-machined element 18 is formed exclusively by the lateral etching of an N+ buried layer 12, in accordance with the process shown in Figures 2a to 2c. The cantilevered beam terminates in a large deflectable accelerometre mass 32 which is also surrounded by the narrow trench 20b and suspended over the cavity 22. The motion-sensing device 25 further includes conventional features, such as metal electrodes 30 and a pair of N-epitaxial regions 26 which are isolated from the remainder of the substrate 10 by a combination of trench and ~~P+ junction isolation 28.~~

As a result of the chlorine plasma-etching process of this invention, the motion-sensing device 25 illustrated in Figure 3 can be fabricated with cantilevered beams having a width of as little as about 1 micrometre and an accelerometre mass area of as little as 100 $\mu m^2$. Such an extremely small motion-sensing device 25 enables one-chip accelerometres to be fabricated more easily alongside their corresponding integrated control circuits. It will be apparent to those skilled in the art that numerous other suspended-mass configurations are possible.

With additional processing steps, various other types of sensing devices can be fabricated using the method of this invention. Figures 4a to 4c demonstrate how a pressure-sensing membrane 38 can be fabricated by sealing the cavity 22 from the surface of the epitaxial layer 14 with a thin silicon membrane. In accordance with this invention, the additional processing requir s only one additional masking step beyond conventional integrated circuit processing, and involves a novel method of sealing the trenches 20 with a polysilicon layer 36, such that the polysilicon layer 36 completely plugs the trenches 20.

Illustrated in Figures 4a to 4c is a piezoresistor 34 which can be formed in any conventional manner to serve as the sensing element for the pressure-sensing membrane 38, which is composed of the epitaxial layer 14, the polysilicon layer 36, and the oxide layer 16. As shown, the piezoresistor 34 is a diffused piezoresistor formed in the epitaxial layer 14 in accordance with known methods. However, for a higher temperature capability, it may be preferable that the piezoresistor 34 should be a polysilicon piezoresistor (not shown) which can be fabricated from the polysilicon layer 36 by performing an additional mask and implant, as will be noted where appropriate below.

The piezoresistor 34, as well as the integrated sensor control circuits (not shown) for the pressure-sensing membrane 38, can be formed on the same epitaxial layer 14 using standard integrated circuit processing. Because only one additional masking level is required to perform the bulk micro-machining process of this invention, such integrated circuit processing can be completed prior to formation of the trenches 20 and the cavity 22. Otherwise, the preferred method for forming the pressure-sensing membrane 38 shown in Figures 4a to 4c begins with the preferred bulk micro-machining process of this invention.

In the discussion that follows, the trenches are designated as being circular, closely-spaced trenches 20a having a diametre of less than about 2 micrometres, so as to be able to later distinguish their columnar shape from other trench shapes. Those skilled in the art will recognise that the circular shape of the trenches 20a is not a design requirement, but is depicted only for illustrative purposes. Otherwise, the cavity 22 and silicon oxide layer 16 shown in Figure 4a are essentially identical to that shown in Figure 2c for the description of the preferred bulk micro-machining process.

Once the cavity 22 and the circular trenches 20a are formed, the layer of polysilicon 36 is deposited on the silicon oxide layer 16 to a thickness of about 2 micrometres using any known method, such as a chemical vapour deposition process. As shown in Figure 4b, the polysilicon 36 enters the circular trenches 20a and the cavity 22 so as to hermetically seal the cavity 22 from the surface of the epitaxial layer 14. In a preferred embodiment, the polysilicon 36 is deposited in a vacuum such that the cavity 22 is sealed under vacuum to enhance its pressure-sensing capability. The pressure-sensing membrane 38 is completed by etching back the polysilicon layer 36 from the silicon oxide layer 16, using a standard plasma-etch end-point technique so as to leave the polysilicon 36 within the circular trenches 20a and the cavity 22.

The oxide layer 16 is then stripped and a second oxide layer 16a is formed, as shown in Figure 4c.

Prior to etching back the polysilicon layer 36, the aforementioned polysilicon piezoresistor (not shown), as well as numerous other active integrated circuit devices such as polysilicon MOS gates and polysilicon resistors, can be fabricated from the polysilicon layer 36 in accordance with the following procedure. First, the polysilicon layer 36 is appropriately doped and a portion of the doped polysilicon layer 36 is masked so as to define the desired device or devices. The exposed areas of the polysilicon layer 36 are then etched from the surface of the oxide layer 16, the masking material is removed, and the dopant in the remaining polysilicon layer is activated in a known manner so as to form an active integrated semiconductor device. Whilst the formation of a polysilicon device as described above is an optional feature of this invention, such a capability is a highly advantageous secondary benefit which is made possible by the preferred processing method illustrated in Figures 4a to 4c.

A fundamental benefit to the preferred processing method of this invention lies in the manner in which the cavity 22 is created. Because the cavity 22 can be formed with rounded corners as a result of the preferred bulk micro-machining process, in contrast to the sharp corners which are formed using current stacked wafer fabrication techniques, the pressure-sensing membrane 38 described above is able to substantially avoid stress concentrations associated with such sharp corners and edges. As a result, the piezoresistor 34 is more likely to be in a uniform stress field, such that stresses induced by pressure applied to the surface of the pressure-sensing membrane 38 will be more accurately detected by the piezoresistor 34. Alignment of the piezoresistor 34 is easier and more precise when the piezoresistor 34 and the cavity 22 are defined from the front surface of the wafer.

As shown in greater detail in Figure 5, the accelerometre mass 32 of Figure 3 can also be advantageously fabricated using the additional polysilicon deposition process of this invention. A trench 20b is used to define the lateral dimensions of the accelerometre mass 32. The selective removal of the silicon oxide layer 16 from those surface regions of the epitaxial layer 14 corresponds to the desired placement of the trenches 20a and 20b, as shown. The bulk micro-machining etch of this invention then proceeds as previously described.

In Figure 5, the circular trenches 20a are differentiated from the elongated trench 20b because each one primarily serves a different function. The circular tr nches 20a promote the lateral etching of the N+ buried layer 12 to form the cavity 22, whilst the elongated trench 20b serves to release the outer edge of the accelerometre mass 32 from the adjacent substrate 10. One skilled in the art will realise that the number and diametre of the circular trenches 20a, as well as the length and width of the elongated trench 20b, may be adjusted to the desired size of the accelerometre mass 32. The size of the circular and elongated trenches 20a and 20b are limited by the ability of the polysilicon deposition process to plug the circular trenches 20a with polysilicon 36, whilst only coating the walls of the elongated trench 20b with the polysilicon 36 such that the accelerometre mass 32 is able to move relative to the substrate 10 in response to an acceleration of the device. Generally, a preferred diametre for the circular trenches 20a is less than about 2 micrometres, while the preferred width of the elongated trench 20b is at least about 5 micrometres. However, different dimensions for the trenches 20a can be produced if openings are desired in the accelerator mass 32 for improved damping behaviour of the micro-machined element.

The technique of forming both narrow circular trenches 20a and wider elongated trenches 20b on the same substrate with the bulk micro-machining and polysilicon deposition processes of this invention facilitates the ability to form two different sensing devices adjacent to each other on the same substrate. An example is shown in Figure 6, in which the pressure-sensing membrane 38 of Figure 4c is formed adjacent the motion-sensing device 25 of Figure 3. Advantageously, in that the bulk micro-machining and polysilicon deposition processes of this invention are compatible with bipolar and BiCMOS processes, integrated circuits 40 associated with the pressure-sensing membrane 38 and the motion-sensing device 25 can be formed immediately adjacent the devices on the same wafer, either before or after the bulk micro-machining or polysilicon deposition processes are performed.

Another example of processing compatibility is illustrated in Figure 7, in which two pressure-sensing membranes 38a and 38b having respective piezoresistors (not shown) are formed in the same substrate 10, but with one membrane 38a being responsive to pressure on the rearside of the wafer, whilst the other membrane 38b serves as a reference for the rearside membrane 38a by detecting pressure only at the front side of the wafer. This arrangement is particularly advantageous in automotive applications, such as where the rearside membrane 38a is exposed to the corrosive environment of an engine manifold to sense manifold pressure, whilst the front side sensor 38b can be isolated from the manifold gases and used to sense atmospheric pressure. Such a capability is in

contrast to the limited capabilities of stacked-wafer techniques and wet-etching techniques currently employed to form semiconductor pressure sensors.

The pressure sensor combination of this invention is made possible by including two additional masking steps. The preferred process begins with using standard integrated circuit processing with a monocrystalline silicon wafer which has been cut so that its top surface lies along a <100> crystallographic plane, as is usual in MOS technology. Preferably, after the last thermal cycle used to form the integrated circuit 40, a silicon etch mask (not shown) is patterned into the thick oxide layer 16 (not shown) previously noted in the description of the bulk micro-machining process of this invention. Two arrays of circular trenches 20a are then etched through the epitaxial layer 14 and into the N+ buried layer 12 (not shown), so as to permit the formation of a cavity 22 under each array of circular trenches 20a using the preferred plasma-etching process of this invention. The circular trenches 20a are each preferably no more than about 2 micrometres in diametre, as noted previously under the discussion for Figures 4a to 4c.

After cleaning the epitaxial layer 14 in any conventional manner, the wafer is oxidised so as to form an oxide layer 42 on the walls of the circular trenches 20a as well as on the interior surfaces of the cavities 22. In accordance with the process step illustrated in Figure 4b, a thick polysilicon layer 36 having a thickness of about 1.5 to about 2 micrometres is then deposited on the wafer so as to plug the circular trenches 20a and thereby seal each of the cavities 22 from the front side of the wafer. The polysilicon layer 36 is then etched back, as previously illustrated in Figure 4c, leaving only the plugs within the circular trenches 20a and the polysilicon layer 36 on the interior surfaces of the cavities 22.

After an optional passivation step, a rearside mask (not shown) is aligned with the membrane 38a and a conventional anisotropic wet silicon etch is performed which preferentially etches the <100> plane to form a rearside trench 44 that extends up to the oxide layer 42 deposited on the surfaces of the cavity 22 corresponding to the membrane 38a. The oxide layer 42 serves to stop this wet-etch process at the bottom of the cavity 22. Next, a buffered hydrofluoric acid etch is employed to etch away the oxide layer 42 at the bottom of the cavity 22, and the polysilicon layer 36 at the bottom of the cavity 22 is then etched using a conventional plasma-etching process so as to vent the cavity 22 to the rearside of the substrate 10. The above processes leave the membrane 38a intact, including the polysilicon layer 36 and the oxide layer 42 on the top of the cavity 22.

With the pressure sensor arrangement of Figure 7, the corrosive manifold environment is exposed only to silicon on the rearside of the wafer. Manifold gases are never exposed to the metal layers, bond pads, wire bonds or solder bumps of the integrated circuit 40, so that protective organic coatings are unnecessary. Similarly, the pressure sensor arrangement of this invention can operate in a highly reliable manner within other corrosive environments in which pressure measurement and comparison of two regions of pressure are required.

Referring to Figures 8a and 8b, an illustrative example of an improved micro-machined silicon capacitor 46 is shown which can be formed in an epitaxial layer 14 with the bulk micro-machining and deposition processes of this invention. The capacitor 46 shown is a parallel plate capacitor, in which the capacitance value of the capacitor 46 is determined by the distance between a pair of capacitor plates 47. These plates 47 can be formed of single crystal silicon, polysilicon, or other suitable materials. As illustrated, the capacitor 46 is defined by a single elongated trench 20b and a cavity 22 which separate the opposing capacitor plates 47. Both the elongated trench 20b and the cavity 22 are formed using the bulk micro-machining process of this invention, in accordance with the process shown in Figures 2a to 2c.

Conventional trench-etching processes are typically capable of creating a gap of no less than about 0.8 to about 1.5 micrometres between the capacitor plates. However, by adopting the additional polysilicon deposition process of this invention, the gap width can be significantly reduced to enhance the capacitance value of the capacitor 46. As shown in Figure 8a, polysilicon 36 is deposited in much the same manner as outlined in Figures 4 and 5, taking note that the width of the elongated trench 20b must be greater than twice the thickness of the deposited polysilicon layer 36 so as to ensure that the trench 20b will not be closed during the deposition process. Afterwards, the polysilicon etch-back described in reference to Figure 4c is performed to produce the capacitor 46 shown in Figure 8b. The etch-back is conducted in a known manner so that the polysilicon 36 remains on the walls of the trench 20b. By making the polysilicon 36 electrically conductive by a suitable method known in the art, the polysilicon layer 36 forms an electrically integral part of the capacitor 46.

Here, the effect of the polysilicon deposition process of this invention is to reduce the spacing between the capacitor plates 47 by twice the thickness of the polysilicon layer 36. As a result, the capacitance value of the capacitor 46 can be more than doubled without the addition of a masking l vel to the integrated circuit proc ssing of the

substrate 10. Whilst polysilicon is preferred for the layer 36, those skilled in the art will recognise that other electrically-conductive materials could be deposited using known techniques instead of the preferred polysilicon. In addition, this method for reducing the plate spacing of a micro-machined capacitor can also be used in other micro-machined devices found in the prior art.

With additional processing steps, further improvements and refinements can be achieved with the various types of sensing devices fabricated using the bulk micro-machining method of this invention. Figures 9a to 9d and 10a to 10c demonstrate how the motion-sensing device 25 of Figure 3 can be encapsulated for purposes of isolating the micro-machined element 18 and the accelerator mass 32 from the environment of the substrate 10. In accordance with this invention, these encapsulation processes can be performed within the wafer clean-room environment, so as to significantly reduce the chance of particles being introduced into regions of the motion-sensing device 25 which may affect the mobility of the micro-machined element 18 or the accelerometre mass 32.

Illustrated in Figures 9a to 9d is a polyimide encapsulation process which employs a sacrificial polyimide layer which may or may not be photodefinable. Though any surface structure or device can be encapsulated using the polyimide encapsulation process feature of this invention, in a preferred embodiment the encapsulation method begins with the bulk micro-machining process of this invention, whereby a micro-machined element 18 is formed so as to be suspended over a cavity 22. The micro-machined element 18 will typically be a cantilevered beam or accelerometre mass, though other motion-sensing members are foreseeable. A photo-sensitive polyimide layer 48 is then spun onto the substrate using known spinning processes, such that the cavity 22 is filled and the micro-machined element 18 is immobilised. The polyimide layer 48 is then masked and developed in a conventional manner to leave the polyimide layer 48 primarily within the cavity 22 and over the adjacent surface of the substrate 10, as shown in Figure 9a.

The polyimide layer 48 is then cured at a temperature of about 400°C for a duration of about one hour, and a film 50 of either silicon nitride or silicon dioxide is then deposited on the device so as to completely cover the polyimide layer 48, as shown in Figure 9b. Low-stress silicon nitride deposited by plasma-enhanced chemical vapour deposition (PECVD) is preferred due to its ability to adhere well to the polyimide layer 48. The silicon nitride film 50 must then be annealed at a temperature of between about 350°C and about 400°C for a duration of about 45 minutes, so as to relieve stress therein and thereby to ensure a high-quality encapsulation chamber. Next, several holes 52 are photo-patterned in a conventional manner in the silicon nitride film 50 to expose the polyimide layer 48 which overlays the adjacent substrate 10, as shown in Figure 9c. The polyimide layer 48 is then completely removed using a conventional wet chemical or plasma oxygen etch through the openings 52 in the silicon nitride film 50, so as to permit movement of the micro-machined element 18 within the enclosure formed by the silicon nitride film 50. An additional plasma silicon nitride film 54, or any other suitable film such as silicon dioxide or an organic material, is then applied so as to either plug or cover the openings 52 in the first silicon nitride film 50 and thus encapsulate the micro-machined element 18, as shown in Figure 9d.

Those skilled in the art will recognise that a wide variety of microstructures can be encapsulated with this technique. Therefore, the disclosures of this feature of the invention are not limited solely to the encapsulation of the motion-sensing device 25 shown.

Illustrated in Figures 10a to 10c is a second encapsulation process feature of this invention, in which the bulk micro-machining process illustrated in Figures 2a to 2c is employed to both define the cavity 22 and the micro-machined element 18, as well as to form a bulk silicon encapsulating structure. This encapsulation process differs from the process of Figures 2a to 2c in that, in addition to the first N+ buried layer 12, second and third N+ buried layers 58 and 60, respectively, are formed in the epitaxial layer 14, as seen in Figure 10b.

Most preferably, the second N+ buried layer 58 is formed by first forming an N+ region (corresponding to the third N+ buried layer 60) in the surface of the first epitaxial layer 14, and then further doping a portion of this N+ region above a portion of the first N+ buried layer 12. The first and third N+ buried layers 12 and 60 are preferably doped with arsenic ions because arsenic diffuses relatively slowly in silicon, whilst the second N+ buried layer 58 is preferably doped with phosphorus ions because phosphorous diffuses relatively quickly in silicon. A second epitaxial layer 56 is then grown over the third N+ buried layer 60, followed by the oxide layer 16. The substrate 10 is then heat-treated sufficiently to diffuse a portion of the dopant of the second N+ buried layer 58 into a portion of the first N+ buried layer 12, as shown in Figure 10b. Importantly, the heat treatment is carried out so that the dopant of the first N+ buried layer 12 does not diffuse into any portion of the third N+ buried layer 60 and, likewise, the dopant of the third N+ buried layer 60 does not diffuse into any portion of the first N+ buried layer 12. As a result, a portion of the first epitaxial layer 14

remains between a portion of the first N+ buried layer 12 and a portion of the third N+ buried layer 60.

The bulk micro-machining process of this invention is then performed to etch several trenches 20 through the second epitaxial layer 56 and into the third N+ buried layer 60, and possibly into the first and second N+ buried layers 12 and 58. As noted before, the preferred chlorine plasma-etching of this invention will preferentially etch the N+ buried layers 12, 58 and 60 so as to form a large cavity 22. Due to the layered arrangement of the N+ buried layers 12, 58 and 60, the cavity 22 will be configured with a lower chamber connected to an upper chamber by an intermediate passage. The micro-machined element 18, shown here as a cantilevered beam, is formed between the upper and lower chambers. The top of the upper chamber and the bottom of the lower chamber can be formed to be at an advantageous distance from the micro-machined element 18 so as to limit the range of movement of the micro-machined element 18.

As shown in Figure 10c, once the micro-machined element 18 has been defined by the preferred plasma-etching process, the trenches 20 formed in the second epitaxial layer 56 can be sealed in accordance with the polysilicon deposition process illustrated in Figures 4a to 4c. After this step, the interior surfaces of the cavity 22 will be coated with an oxide layer 42 and a polysilicon layer 36, in accordance with the preferred features of this invention.

From the above, it can be seen that a wide variety of semiconductor devices can be fabricated with the bulk micro-machining process outlined in Figures 2a to 2c, whilst numerous modifications and enhancements can be realised by further employing the polysilicon deposition process feature of Figures 4 to 8, as well as the encapsulation process features of Figures 9 and 10. Employed alone or in combination, the bulk micro-machining process of this invention makes possible the formation of small integrated sensors which can be incorporated into other integrated circuits. In comparison to conventional sensors fabricated with stacked-wafer techniques or by polysilicon deposition processes, the bulk micro-machining process of this invention is able to fabricate micro-machined elements which do not have the built-in stresses inherent with such prior-art processes as a result of mis-alignment or non-uniform stress distribution. In comparison to conventional wet-etching processes, the bulk micro-machining process of this invention is able to fabricate smaller precision micro-machined elements. In comparison to other bulk micro-machining processes, such as that disclosed by Zhang and McDonald, the bulk micro-machining process of this invention is able to achieve essentially the same advantageous results in fewer processing steps.

According to this invention, the preferred chlorine plasma-etching, when performed under the prescribed conditions, will preferentially etch the N+ buried layer or layers within a silicon wafer, such that the silicon substrate surrounding the N+ buried layer is substantially unaffected. As a result, the size and shape of the cavity or cavities formed can be accurately defined by appropriately defining the size and shape of the corresponding N+ buried layer or layers. Consequently, the bulk micro-machining process of this invention enables a micro-machined element to be accurately predetermined and configured, resulting in a more accurate sensing device.

It should also be noted that, although the advantages associated with the polysilicon deposition and encapsulation process features of this invention are most apparent when used in conjunction with the bulk micro-machining process of this invention, it is foreseeable that each of these inventive processes could be used alone or in conjunction with other bulk micro-machining processes. Furthermore, each of the processes taught herein could also be employed in conjunction with other integrated circuit processes to fabricate semiconductor devices other than the pressure-sensing and motion-sensing devices described.

Therefore, whilst the present invention has been described in terms of a preferred embodiment thereof, it is apparent that other forms could be adopted by one skilled in the art. Accordingly, the scope of the present invention is to be limited only by the scope of the following claims.

The disclosures in United States patent application no. 059,222, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

## Claims

1. A method for micro-machining a surface of a silicon substrate (10) so as to form a semiconductor device therein, characterised in that the method comprises the steps of: forming an N+ region (12) in the surface of the substrate (10); growing an epitaxial silicon layer (14) over the surface of the substrate (10) so as to form an N+ buried layer (12) beneath the surface of the epitaxial silicon layer (14); etching at least one trench (20) through the epitaxial silicon layer (14) and into the N+ buried layer (12); and laterally etching a cavity (22) beneath the surface of the epitaxial silicon layer (14), the lateral etching step being conducted with a chlorine-containing gas at a predetermined

pressure and with the substrate (10) at a predetermined temperature so as to preferentially etch the N+ buried layer (12); whereby a micro-machined element (18) is formed between the cavity (22) and the surface of the epitaxial silicon layer (14), the micro-machined element (18) being a component of the semiconductor device.

2. A method according to claim 1, in which the lateral etching step is conducted at a pressure of 13 Pa (100 mTorr) to about 133 Pa (1000 mTorr) and with the substrate (10) at a temperature of at least 35 °C.

3. A method according to claim 1, which further comprises the step of sealing the trench (20) with a polysilicon film (36) such that the cavity (22) is sealed from the surface of the epitaxial silicon layer (14), the cavity (22) forming a sealed reference chamber for a pressure-sensing device (38)

4. A method according to claim 1, in which the etching step forms a second trench (20) through the epitaxial silicon layer (14) and into the N+ buried layer (12), and in which the method further comprises the step of sealing the second trench (20) with a polysilicon film (36) such that the micro-machined element (18) forms a membrane for a pressure-sensing device (38).

5. A method according to claim 1, in which the etching step forms the trench as an elongated trench (20b) which extends through the epitaxial silicon layer (14) and into the N+ buried layer (12) so as to form the micro-machined element (18) as a cantilevered beam which extends over the cavity, the cantilevered beam defining a suspended mass for a motion-sensing device (25).

6. A method according to claim 1, in which the etching step forms a second trench (20) through the epitaxial silicon layer (14) and into the N+ buried layer (12) such that the micro-machined element (18) is a bridge over the cavity (22)

7. A method according to claim 1, in which the etching step forms at least two elongated trenches (20b) which extend through the epitaxial silicon layer (14) and into the N+ buried layer (12), the elongated trenches (20b) defining the micro-machined element (18) as a mass which is suspended by at least two beams over the cavity (22)

8. A method according to claim 1, in which the etching and lateral etching steps form a capacitor (46) such that the trench (20b) defines opposing plates (47) of the capacitor (46); and the method further comprises the steps of: depositing a conductive film (36) on the opposing plates (47) of the capacitor (46) so as to reduce the distance between the opposing plates (47); and etching back the conductive film (36) so as to isolate the opposing plates from each other; whereby the capacitance value of the capacitor (46) is increased.

9. A method according to claim 1, which further comprises the steps of: forming an oxide layer (16) on the epitaxial silicon layer (14) prior to etching the trench (20a); applying a polysilicon layer (36) on a surface of the oxide layer (16) after etching the trench (20a); doping the polysilicon layer (36) with a dopant; masking a predetermined region of the polysilicon layer (36) with a masking material; etching exposed portions of the polysilicon layer (36) from the surface of the oxide layer (16) so as to leave at least one remaining polysilicon region on the oxide layer (16); removing the masking material; and activating the dopant in the remaining polysilicon region; whereby the remaining polysilicon region defines an active integrated circuit device (34)

10. A method according to claim 1, which further comprises the steps of: filling the cavity (22) and the trench (20) with polyimide (48) such that the micro-machined element (18) is substantially immobilised; depositing over the polyimide (48) a first layer of a material (50) selected from the group consisting of silicon nitride and silicon dioxide; annealing the first layer of material (50) at a temperature and for a duration which are sufficient to relieve stress in the first layer of material (50); forming at least one opening (52) in the first layer of material (50); etching the polyimide (48) through the opening (52) in the first layer of material (50) so as to release the micro-machined element (18); and depositing over the first layer of material (50) a second layer of a material (54) so as to seal the opening (52) in the first layer of material (50) and to form an encapsulating layer over the micro-machined element (18); whereby the micro-machined element (18) is free to respond to motion of the substrate (10) whilst being protected by the encapsulating layer (54)

11. A method according to claim 1, in which the N+ buried layer (12) is a first N+ buried layer

formed by doping the substrate (10) with an n-type species which diffuses relatively slowly in silicon, and wherein the epitaxial silicon layer (14) is a first epitaxial silicon layer, and the method further comprises the steps of: forming a second N+ region (60) in the surface of the first epitaxial silicon layer (14) by doping a region of the first epitaxial silicon layer (14) with an n-type species which diffuses relatively slowly in silicon; forming a third N+ region (58) within a portion of the second N+ region (60) and above a portion of the first N+ buried layer (12), the third N+ region (58) being doped with an n-type species which diffuses relatively quickly in silicon; growing a second epitaxial silicon layer (56) over the surface of the first epitaxial silicon layer (14) so as to establish second and third N+ buried layers (58,60) beneath the surface of the second epitaxial silicon layer (56) and above the first N+ buried layer (12); heat-treating the substrate (10) sufficiently to diffuse a portion of the n-type species of the third N+ buried layer (58) into a portion of the first N+ buried layer (12), the heat treatment being insufficient to diffuse the n-type species of the first N+ buried layer (12) into any portion of the second N+ buried layer (60) and being insufficient to diffuse the n-type species of the second N+ buried layer (60) into any portion of the first N+ buried layer (12), so that a portion of the first epitaxial silicon layer (14) remains between a portion of the first N+ buried layer (12) and a portion of the second N+ buried layer (60); etching at least one trench (20) through the second epitaxial silicon layer (56) and into at least one of the first, second and third N+ buried layers (12,60,58); and laterally etching a cavity (22) beneath the surface of the second epitaxial silicon layer (56), the lateral etching step being conducted with a chlorine-containing gas at a predetermined pressure and with the substrate at a predetermined temperature so as to preferentially etch the first, second and third N+ buried layers (12,60,58); whereby a micro-machined element (18) is formed between an upper portion of the cavity (22) and a lower portion of the cavity (22), the micro-machined element (18) being a component of the semiconductor device.

12. A method according to claim 1, for micro-machining a surface of said silicon layer (14) so as to form a sensing device (38) in the same layer (14) as at least one semiconductor device (40), the method comprising the steps of: etching a plurality of trenches (20a) through the layer (14) so as to laterally etch said cavity (22) beneath the surface of the layer (14); forming an oxide layer (42) on the layer (14) and on the surfaces defined by the trenches (20a) and the cavity (22); and depositing a polysilicon layer (36) over the oxide layer (42) so as to seal the trenches (20a), such that the cavity (22) is a sealed cavity beneath the surface of the layer (14); whereby the micro-machined element is formed between the sealed cavity (22) and the surface of the layer (14), the micro-machined element being a component of the sensing device (38).

13. A method according to claim 12, in which the semiconductor device (40) is formed on the layer (14) after the sensing device (38) has been formed.

14. A method according to claim 12, in which the semiconductor device (40) is formed on the layer (14) prior to the sensing device (38) being formed.

15. A method according to claim 12, in which the lateral etching step forms at least two cavities (22) beneath the surface of the layer (14)

16. A method according to claim 15, in which the step of depositing the polysilicon layer (36) seals at least one of the cavities (22) to form a sealed reference chamber beneath the surface of the layer (14), so that at least another one of the cavities (22) remains vented to a surface of the substrate (10), each one of the cavities (22) forming pressure-reference chambers for the sensing device (38a,38b)

17. A method according to claim 16, in which the sealed reference chamber (22) is sealed under a vacuum.

18. A method according to claim 15, in which the step of depositing the polysilicon layer (36) seals each of the two cavities (22) so as to form two sealed reference chambers for the pressure-sensing device (38).

19. A method according to claim 15, in which the step of depositing the polysilicon layer (36) seals each of the two cavities (22) at the surface of the layer (14), the method further comprising the step of: masking an opposite surface of the substrate (10); etching the opposite surface of the substrate (10) so as to etch the substrate (10) to the oxide layer (42) formed on a first of the two cavities (22); etching through the oxide layer (42) of the first of the two cavities (22) to the polysilicon layer (36)

deposited on the first of the two cavities (22); and etching the polysilicon layer (36) of the first of the two cavities (22) so as to vent the first of the two cavities (22) to the opposite surface of the substrate (10); whereby the first of the two cavities forms a first sensing device (38a) for sensing pressure at the opposite surface of the substrate (10) and the other of the two cavities forms a second sensing device (38b) for sensing pressure at the surface of the layer (14), such that the first and second sensing devices (38a,38b) serve as pressure-references to each other.

**20.** A method according to claim 19, in which the step of etching the opposite surface of the substrate (10) is a wet silicon etch.

**21.** A method according to claim 19, in which the step of etching the opposite surface of the substrate (10) is an anisotropic etch.

**22.** A method according to claim 11, in which the first and second N+ buried layers (12,60) are each doped with arsenic and the third N+ buried layer (58) is doped with phosphorus.

**23.** A pressure-sensing device (38a,38b) formed in a substrate (10,14) having at least one semiconductor device (40) formed thereon for monitoring the pressure-sensing device (38a,38b), the pressure-sensing device (38a,38b) comprising: a first cavity (22) formed beneath a first surface of the substrate (10,14); first pressure-sensing means (38b) formed between the first cavity and the first surface of the substrate (10,14) so as to sense the pressure at the first surface of the substrate; a second cavity (22) formed beneath the first surface of the substrate (10,14) so as to be adjacent the first cavity, the second cavity being vented to a second surface of the substrate; and second pressure-sensing means (38a) formed between the second cavity (22) and the first surface of the substrate (10,14) so as to sense the pressure at the second surface of the substrate; whereby the first and second pressure-sensing means (38a,38b) serve as pressure references to each other.

**24.** A pressure-sensing device (38a,38b) according to claim 23, in which the first surface is a front side of the substrate (10,14) and the second surface is a rearside of the substrate (10,14)

**25.** A pressure-sensing device (38a,38b) according to claim 23, in which the first and second cavities (22) each comprise: an oxide lay r (42) formed on the interior surface of the respective cavity (22); and a polysilicon layer (36) formed over the oxide layer (42) so as to seal the respective cavity (22) from the first surface of the substrate (10,14).

**26.** A pressure-sensing device (38a,38b) according to claim 23, in which a portion of the first surface of the substrate is exposed to atmospheric pressure whilst a portion of the second surface of the substrate is exposed within a manifold of an internal combustion engine, so that the first pressure-sensing means (38b) senses atmospheric pressure and the second pressure-sensing means (38a) senses manifold pressure within the internal combustion engine.

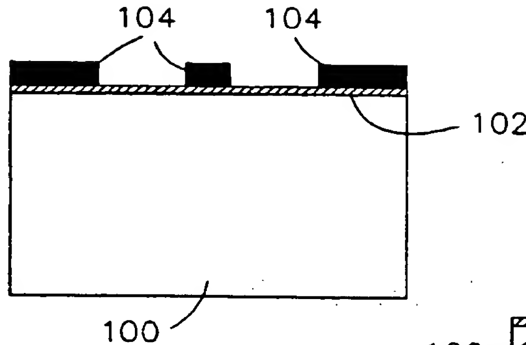



FIG. 1a
PRIOR ART

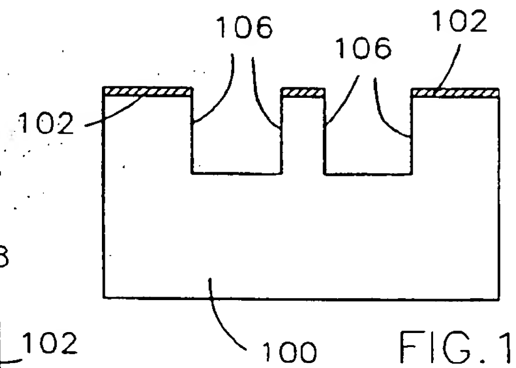



FIG. 1b
PRIOR ART

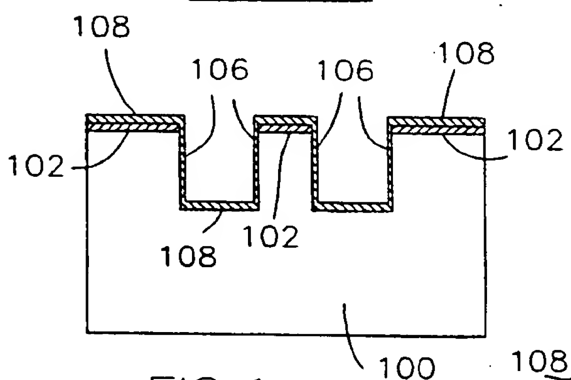



FIG. 1c
PRIOR ART

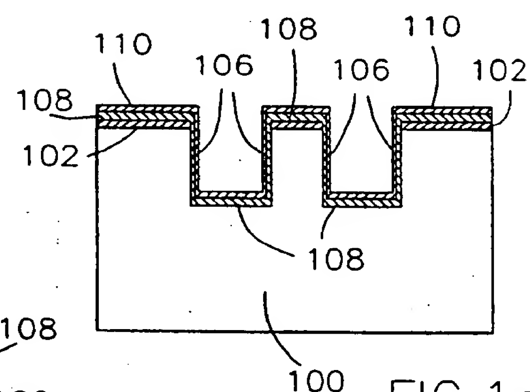



FIG. 1d
PRIOR ART

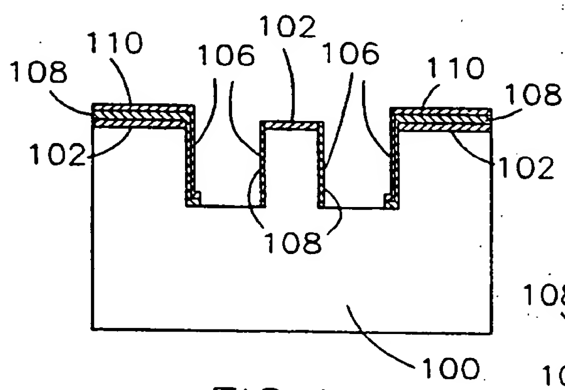



FIG. 1e
PRIOR ART

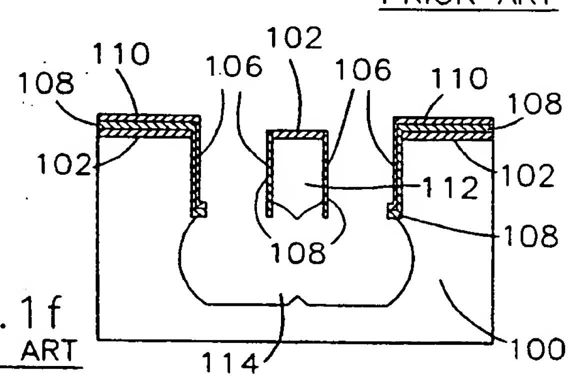



FIG. 1f
PRIOR ART

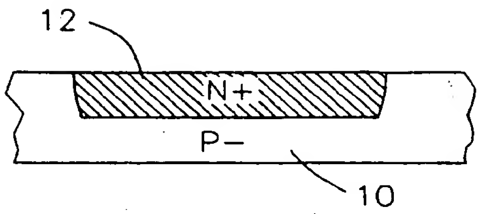



FIG.2a

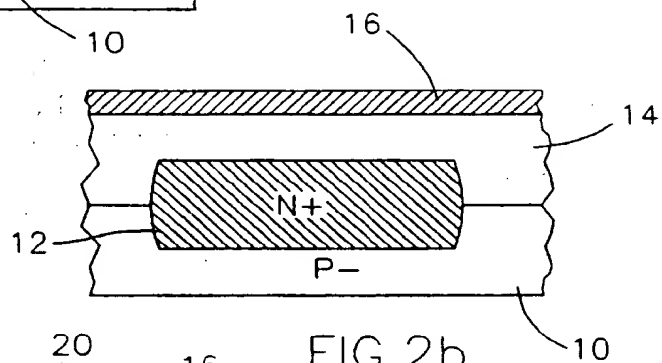



FIG.2b

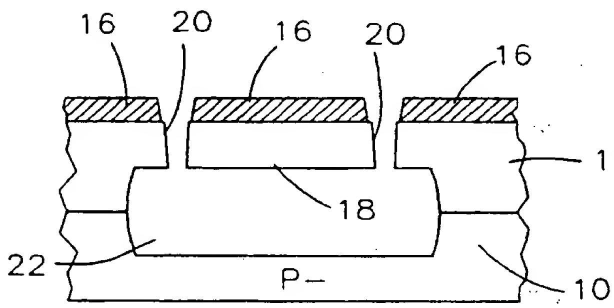



FIG.2c

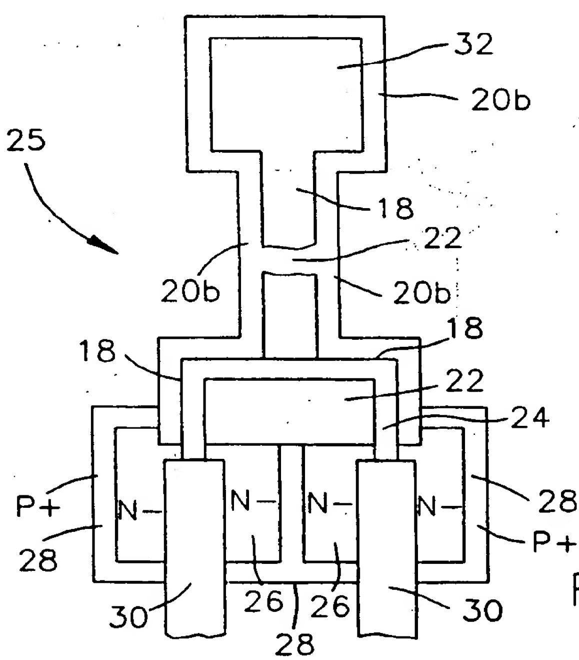



FIG.3

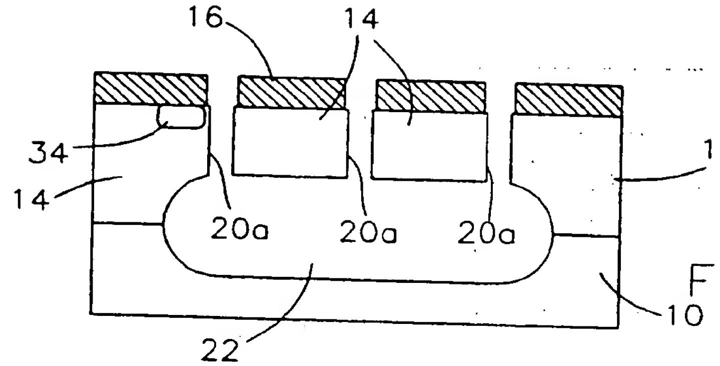



FIG.4a

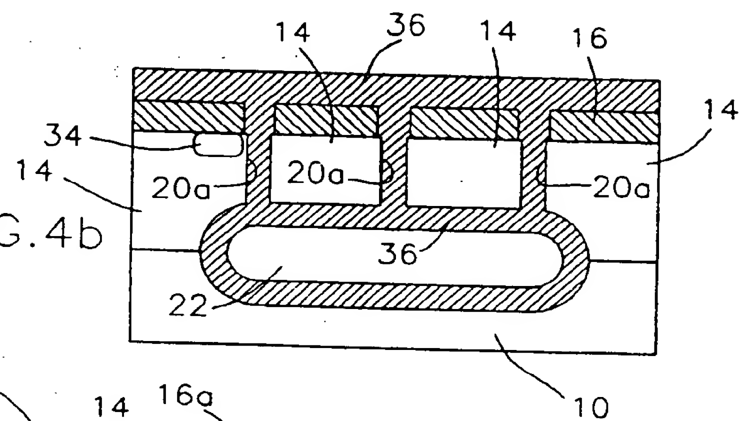



FIG.4b

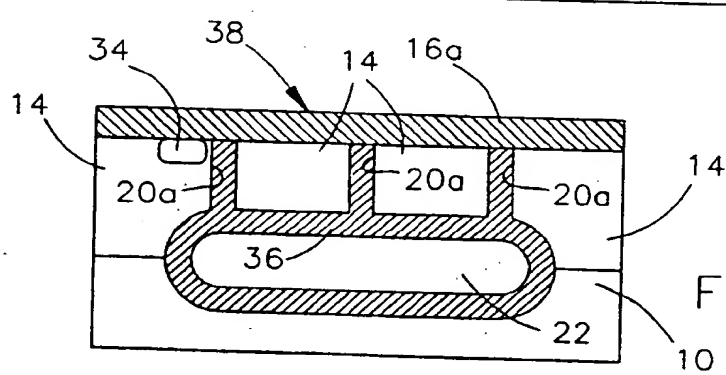



FIG.4c

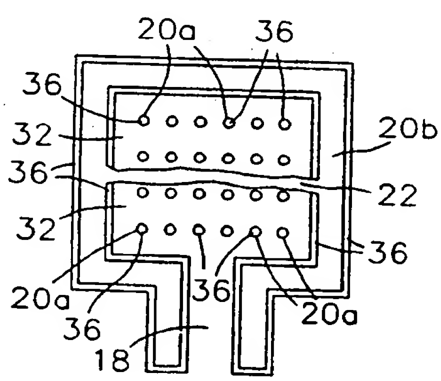



FIG.5

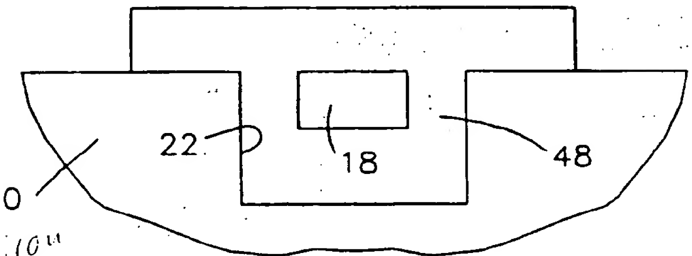
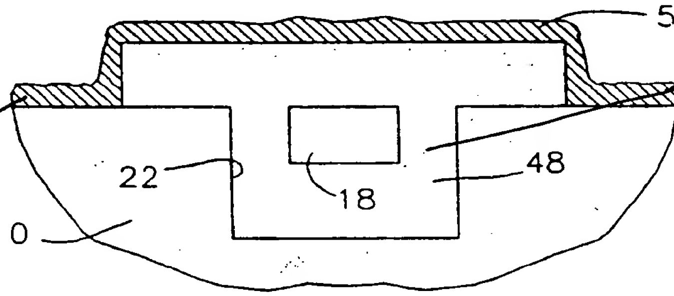



FIG.9a

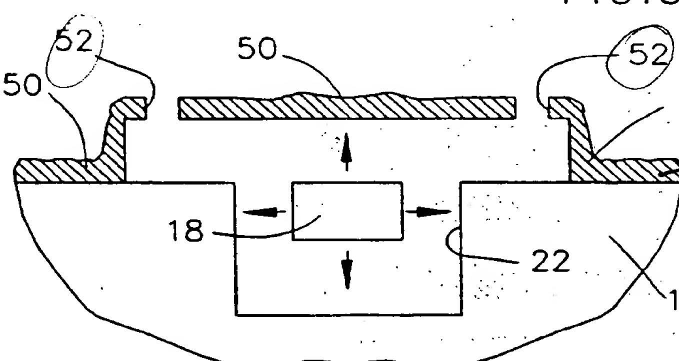
Bulk micro-machining silicon




polyimide

$SiN_3$
$SiO_2$

FIG.9b




Silicon Nitride
Silicon Dioxide

FIG.9c

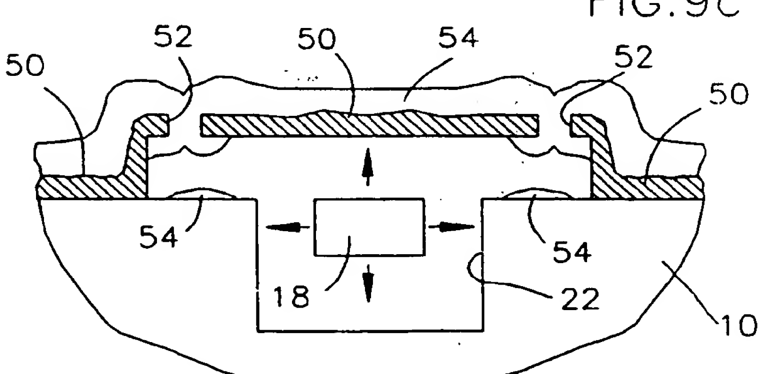



FIG.9d

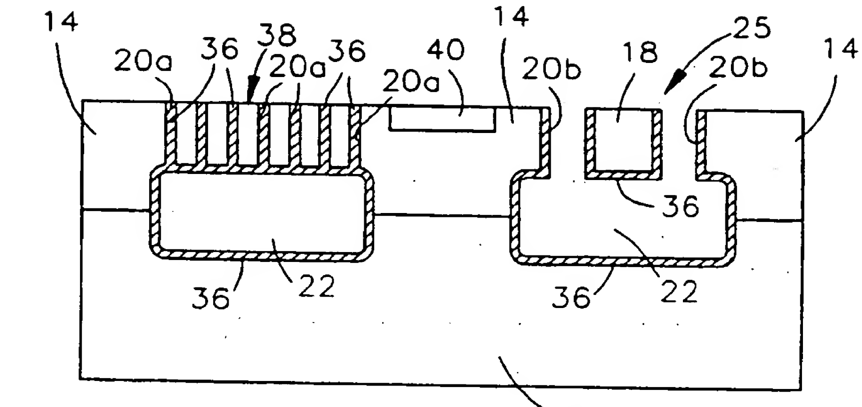



FIG.6

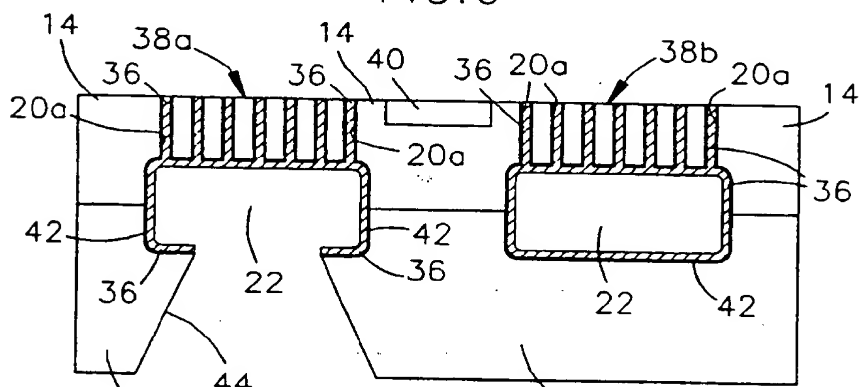



FIG.7

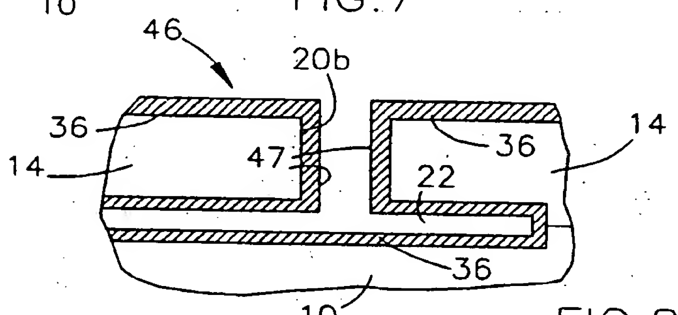



FIG.8a

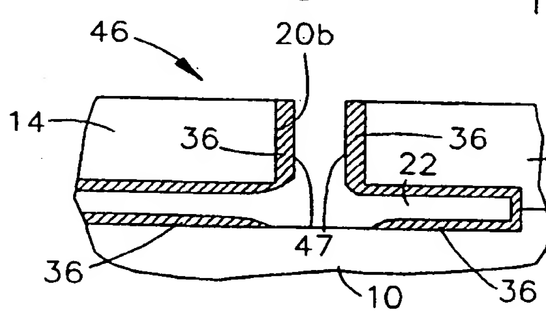



FIG.8b

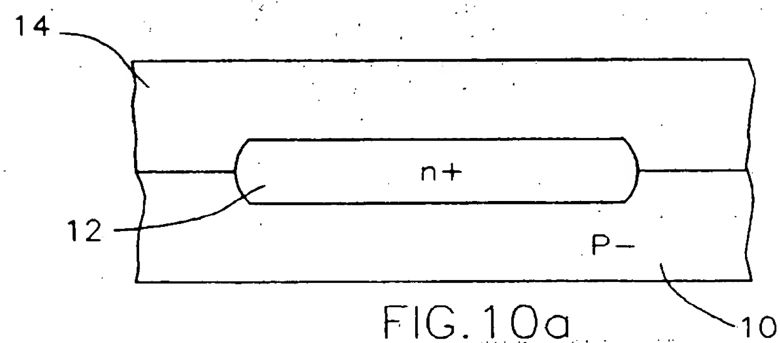



FIG. 10a

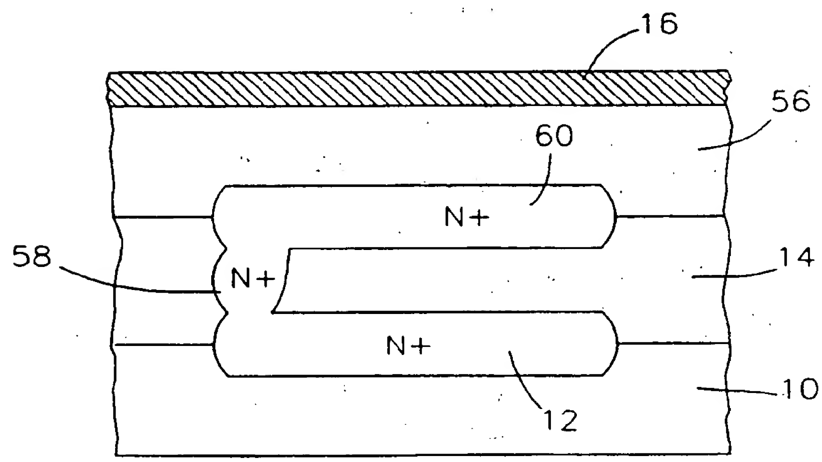



FIG. 10b

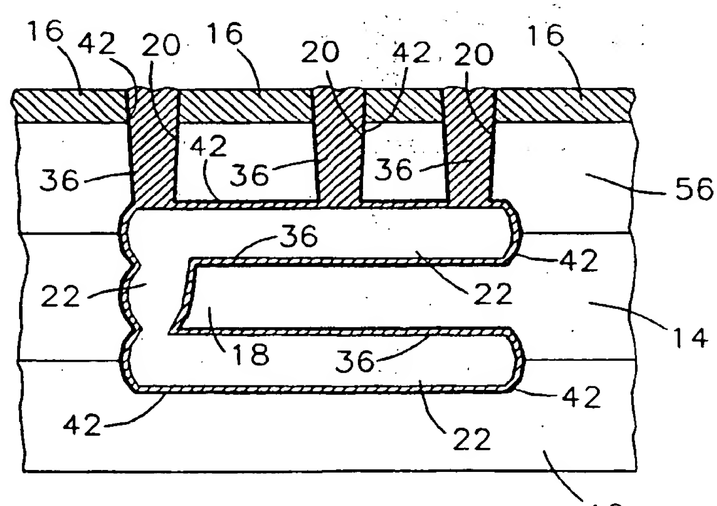



FIG. 10c

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